

Graph Neural Networks and Arithmetic Circuits

Laura Strieker

Paper by:

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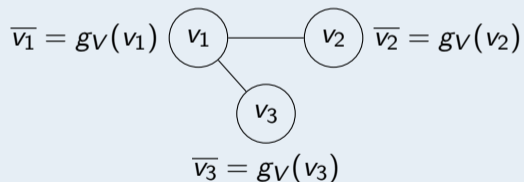
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03.03.25

Preliminaries

Labeled graph

- ▶ Undirected Graph $\mathcal{G} = (V, E, g_V)$ with labeling function $g_V : V \mapsto \mathbb{R}^k$
- ▶ Vectors belonging to nodes, called *feature vectors*



Definition

An L layer *aggregate combine graph neural network* (AC-GNN) is a tuple $\mathcal{D} = (\{\text{AGG}^{(i)}\}_{i=1}^L, \{\text{COM}^{(i)}\}_{i=1}^L, \{\sigma^{(i)}\}_{i=1}^L, \text{CLS})$, where

- ▶ $\{\text{AGG}^{(i)}\}_{i=1}^L$: aggregate functions
- ▶ $\{\text{COM}^{(i)}\}_{i=1}^L$: combine functions
- ▶ $\{\sigma^{(i)}\}_{i=1}^L$: activation functions
- ▶ $\text{CLS}: \mathbb{R}^k \rightarrow \{0, 1\}$: classification function

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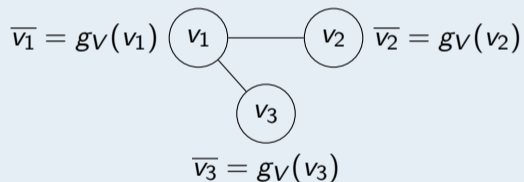
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Updating vectors in every layer $i \leq L$ as follows:

- ▶ initial feature vector of v : $\bar{v}^{(0)} = g_V(v)$
- ▶ for $1 \leq i \leq L$:
 - ▶ $\bar{y} = \text{AGG}^{(i)} \left(\left\{ \left\{ \bar{u}^{(i-1)} \mid u \in N_{\mathcal{G}}(v) \right\} \right\} \right)$
 - ▶ $\bar{v}^{(i)} = \sigma^{(i)} \left(\text{COM}^{(i)} \left(\bar{v}^{(i-1)}, \bar{y} \right) \right)$

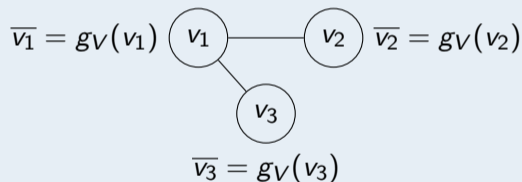
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Labeled graph

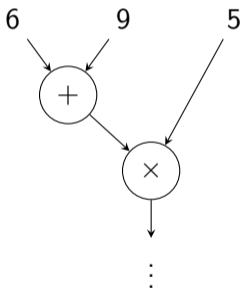
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$$\bar{v}_1^{(i)} = \sigma^{(i)} \left(\text{COM}^{(i)} \left(\bar{v}_1^{(i-1)}, \text{AGG}^{(i)} \left(\left\{ \bar{v}_2^{(i-1)}, \bar{v}_3^{(i-1)} \right\} \right) \right) \right)$$

Definition

Directed acyclic graph with gates that perform arithmetic operations over \mathbb{R}^k .

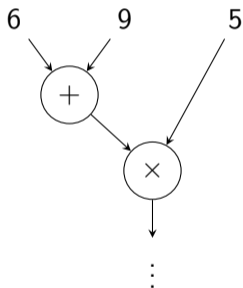


Circuit Function Classes

- ▶ $\text{FAC}_{\mathbb{R}^k}^0$: constant depth & polynomial size

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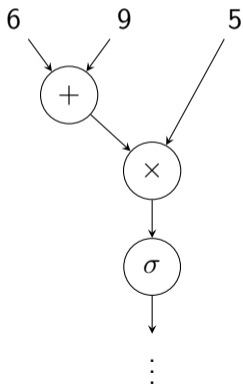
But we want to compare arithmetic circuits to Graph Neural Networks.
How to deal with activation functions?

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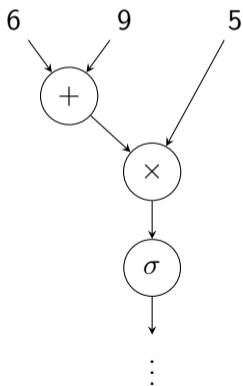


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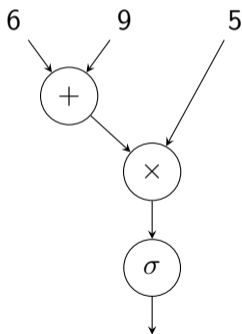


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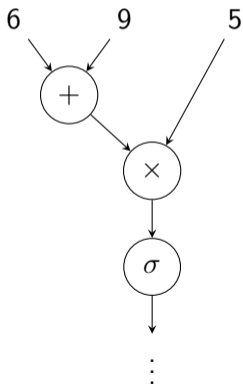
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Nodes in a GNN aggregate the values of their neighbors, regardless of their order. Our circuits should mimic this behavior.

Definition

Directed acyclic graph with gates that perform arithmetic operations over \mathbb{R}^k .



Circuit Function Classes

- ▶ $t\text{FAC}_{\mathbb{R}^k}^0$: constant depth & polynomial size
 - ▶ $t\text{FAC}_{\mathbb{R}^k}^0[\mathcal{A}]$: additional function gates
- t = tailsymmetric*

Graph Neural Networks using Circuits

Model of Computation: Circuit-GNN

- ▶ instead of aggregate/combine functions: circuit families of a specific circuit function class \mathfrak{F}
- ▶ defined set of activation functions \mathcal{A}
- ▶ a function assigning a circuit family and activation function for every layer
- ▶ “a GNN with circuits in its nodes”
- ▶ $(\mathfrak{F}, \mathcal{A})$ -GNN, e.g. $(\text{FAC}_{\mathbb{R}}^0, \{id\})$ -GNN

Theorem

Let \mathcal{N} be a $(t\text{FAC}_{\mathbb{R}^k}^0, \{\text{id}\} \cup \mathcal{A})$ -GNN. Then there exists an $\text{FAC}_{\mathbb{R}^k}^0[\mathcal{A}]$ -circuit family \mathcal{C} , such that for all labeled graphs \mathfrak{G} the circuit family computes the same feature vectors as the C-GNN.

- ▶ idea: roll out the circuits to one big one
- ▶ simulate the circuits of each layer
- ▶ use function gates for the activation functions in \mathcal{A}

Goal

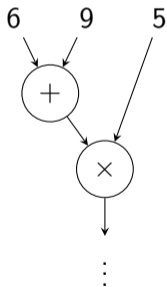
Let $\mathcal{C} = (C_n)_{n \in \mathbb{N}}$ be a circuit family of some circuit function class. Show there exists a C-GNN \mathcal{N} that has the output of the circuit family among its feature vectors.

- ▶ number of layers in $\mathcal{N} = \text{depth of } \mathcal{C}$.
- ▶ use the graph structure of the circuit as the input graph of the C-GNN
- ▶ simulate the computation of the circuit layerwise in the C-GNN and store the intermediate results in the feature vectors

Circuits without additional function gates

Theorem

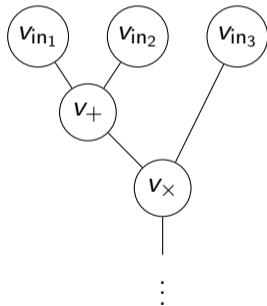
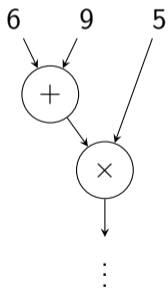
$\text{FAC}_{\mathbb{R}^k}^0$ -circuit family \rightarrow $(t\text{FAC}_{\mathbb{R}^k}^0, \{\text{id}\})$ -GNN



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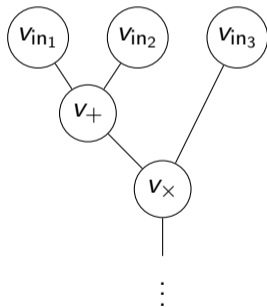
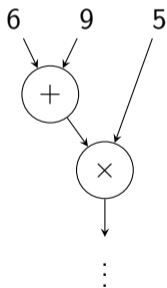
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- ▶ no additional function gates on the circuit side \implies no activation functions needed in the C-GNN (besides identity)

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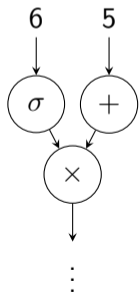
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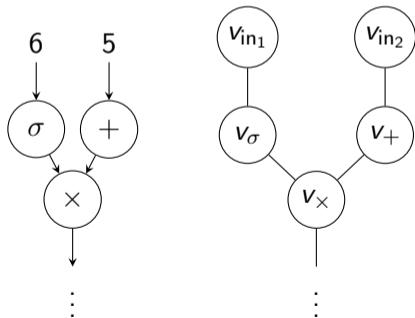


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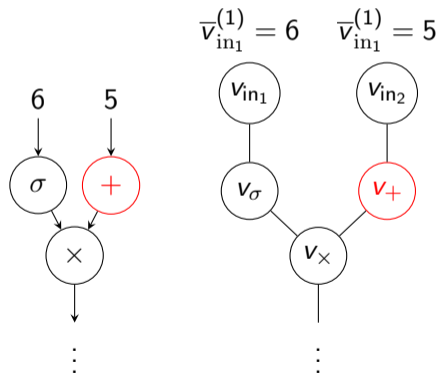


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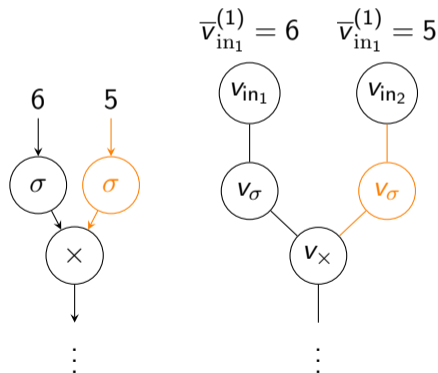


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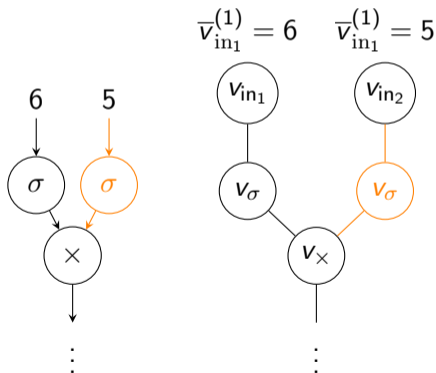


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Thank You